

Appl. No. 09/327,523  
Amdt. Dated September 3, 2004  
Reply to Office Action of March 3, 2004

### REMARKS

In order to overcome the Examiners prior art rejections, Applicants have modified Claim 1 to incorporate the limitations from existing Claim 4, and have now also cancelled Claim 4. Additionally, Applicants have modified Claim 12 to further specify that a negative voltage is applied to a gate of the reset switch. Applicants thank the Examiner for withdrawing the objections to the drawings. In order to overcome the current outstanding objections to Claim 2, Applicants have modified Claim 2, and accordingly Applicants request reconsideration of the objections to Claim 2.

Applicants respectfully request reconsideration of the prior art rejections set forth by the Examiner under 35 U.S.C. §§102 and 103. Applicants respectfully submit that the prior art references of record, whether considered alone, or in combination, fail to either teach or suggest the presently claimed invention. More specifically, Applicants note that in the outstanding Final Office Action, the Examiner has rejected Claim 4 as being obvious in light of the combined teaching of the *Gowda* reference in view of *Miwada*. Applicants note that although *Miwada* does disclose that the transistor designated Tr2 is a depression type transistor, this transistor is absolutely not the reset transistor. As is clearly shown in Figure 1 of *Miwada*, the transistor designated Tr2 is in a source follower circuit located at the output which is not used for resetting purposes. Rather, in contrast with the assertions of the Examiner, it is the transistor designated 8 in the center of the figure, that resets floating diffusion region 7. See Column 4 at lines 43-50. There is no disclosure or even suggestion in *Miwada* that transistor designated 8 is a depression type transistor. Accordingly, the rejection

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set forth by the Examiner must fail because neither *Miwada* nor *Gowda* provides the requisite teaching or suggestion to result in the claimed subject matter.

Additionally, in regard to modified Claim 12, Applicants note that neither *Gowda* nor *Miwada* provide any teaching or suggestion regarding the application of a negative voltage to the gate of a reset switch. See specifically modified Claim 12.

Accordingly, in light of the foregoing, because the references cited by the Examiner fail to provide any teaching or suggestion regarding the selection of pixels in units of rows by controlling a reset potential, Applicants respectfully request that the Examiner now withdraw the rejections and allow all claims in the application.

Respectfully submitted,

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